LXF31K18

Eight channels 310 Msps ADC with 16-bits resolution

A combination of eight analog to digital converter channels and a Xilinx Kintex Ultrascale makes the LXF31K18 the ideal platform for embedded signal processing applications such as Electronic Warfare, Radar receiver, instrumentation or MIMO communication applications. The LXF31K18 is fully compliant to the Vita65.0 openVPX standard and the VITA46.11 VPX shelf management standard.

Analog input

Depending on the application requirements it is possible to order the LXF31K18 with either a DC coupled or an AC coupled analog front end. The DC coupled interface is meant for signal acquisitions in the first Nyquist zone while the AC coupled inputs also offers the option for signal acquisition in the second Nyquist zone.
The ADCs offer 16-bits resolution further contributing to achieve best in class signal to noise ratios.

Clock tree

The onboard low noise clock generator ensures easy integration into small single board systems as well as standalone operation. For larger systems it is possible to easily synchronize multiple boards by providing an external reference clock. This is a special feature offered by the onboard clock pll.

FPGA and Memory

The LXF31K18 comprises a Xilinx Kintex Ultrascale KU060 user programmable FPGA. A majority of the logic, block RAM and all DSP resources are available for customer processing. With the KU060 FPGA the LXF31K18 offers; 663 K logics cells, 1,080 36 Kbit RAM blocs, 3 PCIe interface blocks and 2,760 DSP48 slices. The FPGA speed grade is -2. The LXF31K18 FPGA connects to one 72 bits wide DDR4 memory bank, offering a total of 4GB of storage with error correction codes. At 2400 Mhz the memory bank offers a total bandwidth of 21.6 GB/s. For FPGA configuration the LXF31K18 has a 64MB QSPI FLASH memory.

VPX interface

At the P1 connector the LXF31K18 has two fat pipes that form the data plane. At the expansion plane on P1 there are also two FAT pipes. Each fat pipe can be divided into two thin pipes or four ultra thin pipes. A total of thirty-two user definable LVDS signals connect between the FPGA and the VPX P2 connector. Two types of cooling are supported by the LXF31K18. For the harsher environmental conditions, the board can be ordered in the conduction cooled version. Otherwise the board is available in an air-cooled version.

Key Features:

- **VITA65.0 3U OpenVPX compliant**
- **8 channels ADC**
- **310 MHz ADC update Rate**
- **16-bit Resolution**
- **AC or DC coupled**
- **Flexible clock tree**
- **External Trigger input or output**
- **User programmable Xilinx Kintex Ultrascale KU060 FPGA**
- **4GB DDR4-2400 with ECC**
- **VITA46.11 compliant IPMI Controller**
- **Air cooled or Conduction cooled**

Applications

Systems that will benefit greatly from this product are:

- Radar waveform receivers
- MIMO Applications
- Digital Beam Forming
- Aerospace and test instrumentation
- Telecommunication
- Software defined radio (SDR)

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Specifications

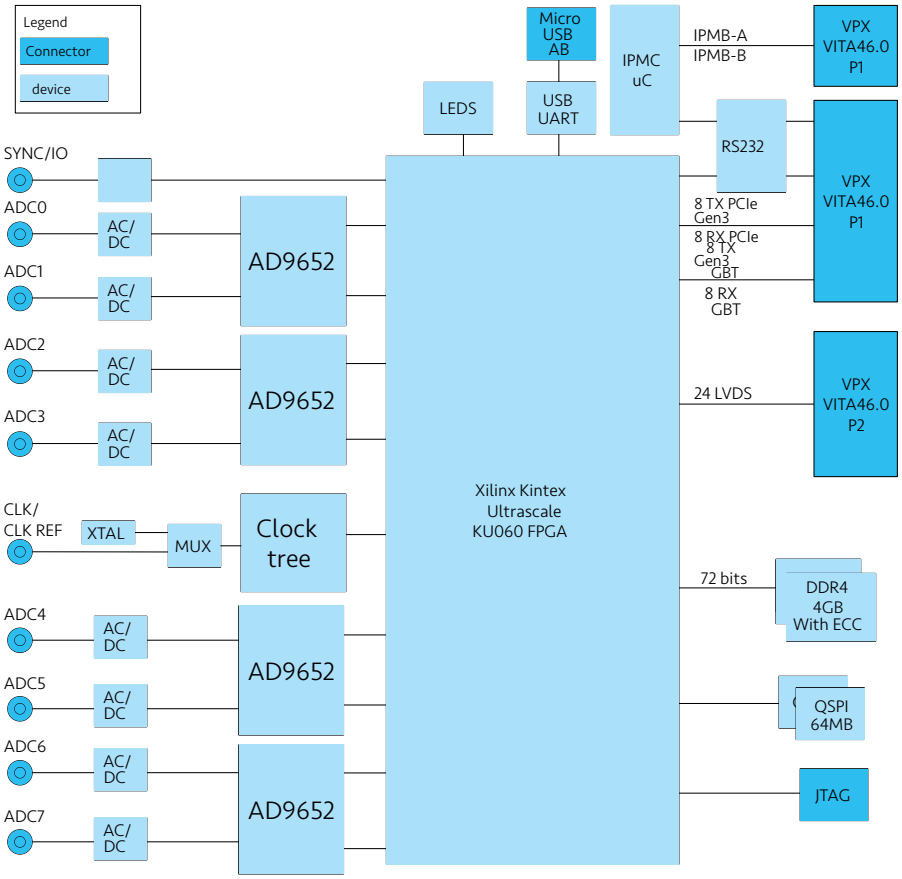
Analog input/output
- AC or DC coupling
- Bandwidth AC 10 MHz -400 MHz
- Bandwidth DC DC - 200 MHz
- AC Full scale input power +6 dBm
- DC Full scale input power +12 dBm
- Impedance 50 Ω
- SSMC or MMCX (default) connector

Analog to Digital Conversion
- FS = Max 310 Gsps
- 16 bits
- SNR @ 70MHz 75 dFs
- SFDR @ 70MHz 87 dBc
- SNR @ 170MHz 73.7 dFs
- SFDR @ 170MHz 85 dBc
- ENOB @ 70MHz 12 bits

FPGA
- Kintex Ultrascale KU060
- XCKU060-1FFVA1156

Memory
- 72 bits DDR4-2400
- 4GB with ECC
- 64MB QSPI FLASH

Support
- Application example for Windows
- Vivado IP integrator IP cores
- Vivado 19.0 support



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