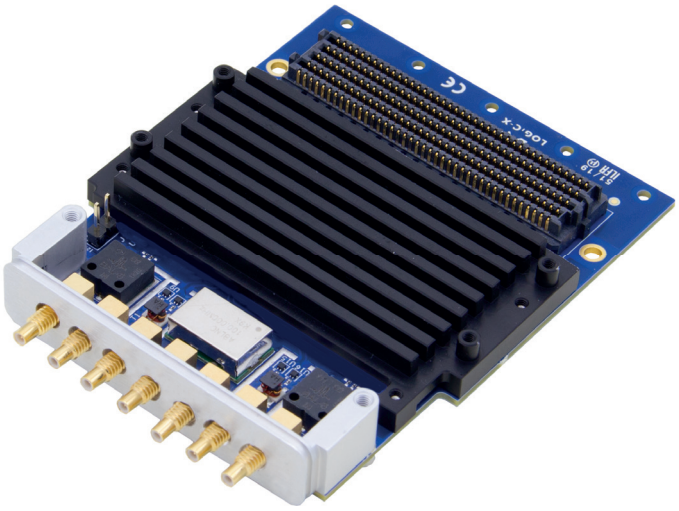


LXD30K0

Single channel 5.4 Gsps ADC and DAC with 12-bits resolution

With the LXD30K0 Logic-X provides a unique analog interface product that is based on the 12-bits low latency wide bandwidth ADC (EV12AS350A) and DAC (EV12DS460) from Teledyne E2V. Multi card synchronization is supported thanks to a flexible clock tree and external synchronization trigger input.

Analog input

With an analog input stage that has a very wide input bandwidth from 0.5 MHz up-to 4.8 GHz and the low latency 5.4 Gsps ADC from E2V (EV12AS350A) the LXD30K0 delivers unmatched performance with regards to SFDR, close in phase noise and latency (7.2 ns) on its analog input channel. Sampling at 5.4 Gsps offers an instantaneous bandwidth of 2.7 GHz.

Analog output

Surpassing the analog input, the analog output offers an even lower latency (1.2 ns) using the EV12DS460 DAC device from E2V. The output bandwidth ranges from 0.5 MHz to 6 GHz and the instantaneous output bandwidth is 1.35 GHz.

12 bit

Both the ADC and DAC offer 12-bits resolution further contributing to achieve best in class signal to noise ratios.

Low Latency

It is possible to achieve a very low latency from the RF input to the RF output because of the LVDS connectivity to the host carrier. This can be less than 18 ns, depending on the carrier that is used.

Clock tree

The onboard low noise clock generator ensures easy integration into small single channel systems as well as standalone operation. For larger systems it is possible to directly provide the sample clock to the front panel SSMC connector or to syn-chronize the local clock generator to an external reference clock.

Applications

Systems that will benefit greatly from this product are:

- Electronic Warfare systems
- Radar waveform generators and receivers
- Advanced digital radio frequency memory (DRFM) sys-tems
- Medical systems
- Telecommunication systems

Key Features:

- FPGA Mezzanine Card (HPC)
- <18 ns RF to RF Latency
- 5.4 GSPS Data Rate
- 12-bit Resolution
- 0.5 to 6000 MHz Bandwidth
- LVDS signaling
- No calibration required
- Flexible clock tree
- External Trigger input and output
- System power saving options
- Advanced power monitoring
- VITA 57.1 and 57.4 compatible

LOGIC-X
THE POWER OF LOGIC

LXD30K0 *Single channel 5.4 Gsps ADC and DAC with 12-bits resolution*

Specifications

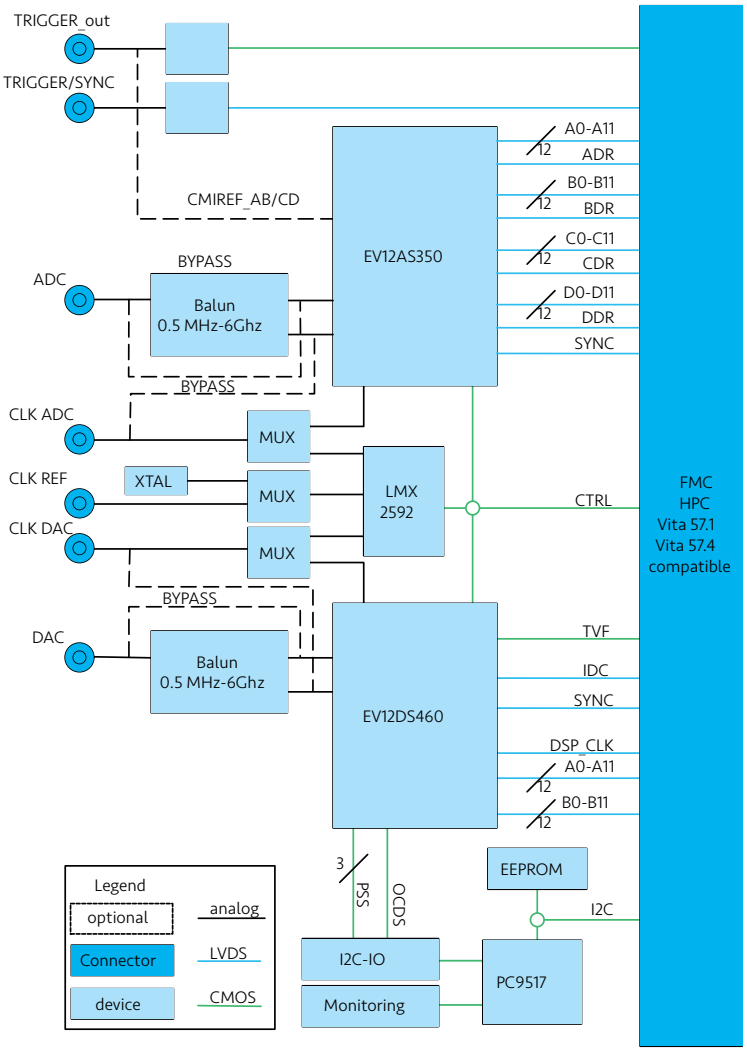
Analog input
- AC coupling (differential DC optional)
- Bandwidth 0.5MHz -4.8 GHz
- Full scale Input power 8.5 dBm
- Impedance 50 Ω
- SSMC connector

Analog output
- AC coupling (differential DC optional)
- Bandwidth 0.5MHz -6 GHz
- Full scale Output power - dBm (NRZ)
- Impedance 50 Ω
- SSMC connector

Analog to Digital Conversion
- FS = Max 5.4 Gsps
- 12 bit
- SNR @ 1GHz 55 dBc
- SFDR @ 1GHz 60.5 dBc
- ENOB @ 1GHz 8.5 bits

Digital to Analog conversion
- FS = Max 5.4 Gsps
- Data rate = Max 2.7 Gsps
- 12 bit
- SFDR @ 1GHz 59 dBc (NRTZ)
- SFDR @ 3GHz 55 dBc (NRTZ

Mechanical
- Vita 57.1 High Pin Count FMC
- Vita 57.4 compatible
- Convection and conduction cooled
- Max 14 Watts
- Several power saving modes
- SSMC connectors



Compatible with LXF90K0

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