



LXD20K0

One channel 5.4 GHz DAC with 12-bits resolution

With the LX20K0 Logic-X provides a unique analog interface product that is based on the 12-bits low latency wide bandwidth DAC (EV12DS460) from Teledyne E2V. Multi card synchronization is supported thanks to a flexible clock tree and external synchronization trigger input.

Analog output

The analog output offers a low latency (1.2 ns) from FPGA to RF using the EV12DS480 DAC device from E2V. The product has an output bandwidth from 0.5MHz to 6GHz. The instantaneous output bandwidth is up-to 1.3 GHz. Thanks to the unique operating modes of the EV12DS460 it is possible to place the signal into the higher Nyquist bands.

12 bit

The DAC offers a 12-bits resolution further contributing to achieve best in class signal to noise ratios.

Low Latency

It is possible to achieve a very low latency from the FPGA to the RF output because of the LVDS connectivity to the host carrier. This can be less than 4 ns, depending on the carrier that is used.

Clock tree

The onboard low noise clock generator ensures easy integration into small single channel systems as well as standalone operation. For larger systems it is possible to directly provide the sample clock to the front panel SSMC connector or to synchronize the local clock generator to an external reference clock.

Applications

Systems that will benefit greatly from this product are:

- Electronic Warfare systems
- Radar waveform generators
- Arbitrary waveform generators
- Advanced digital radio frequency memory (DRFM) systems
- Medical systems
- Telecommunication systems
- Many more

Key Features:

- FPGA Mezzanine (HPC)
- <4 ns FPGA to RF Latency
- 5.4 GHz sample clock
- 5.4 GSPS Data Rate
- 12-bit Resolution
- 0.5 to 6000 MHz Bandwidth
- LVDS signaling
- Flexible clock tree
- External Trigger input and output
- VITA 57.1 and 57.4 compatible



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Specifications

Analog output

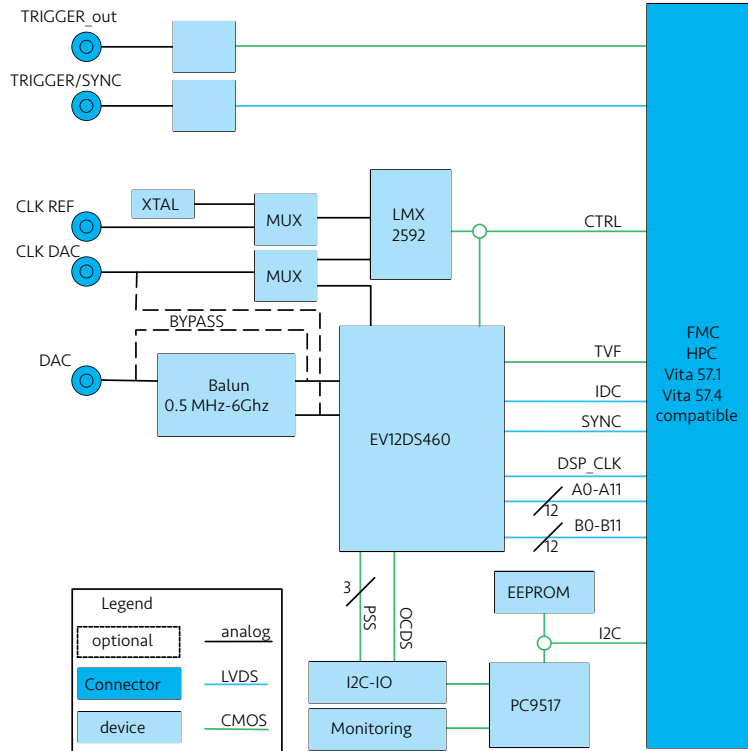
- AC coupling (differential DC optional)
- Bandwidth 0.5MHz –6.0 GHz
- Full scale Output power –5 dBm (NRZ)
- Impedance 50 Ω
- SSMC connector

Digital to Analog conversion

- FS = Max 5.4 Gsp/s
- Data rate = Max 2.7 Gsp/s
- 12 bit
- SFDR @ 1GHz 59 dBc (NRTZ)
- SFDR @ 3GHz 55 dBc (NRTZ)

Mechanical

- Vita 57.1 High Pin Count FMC
- Vita 57.4 compatible
- Convection and conduction cooled
- Max 5 Watts
- Power saving modes
- SSMC connectors



Compatible with LXF90K0



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R&D TOOL FPGA SDR FMC Training DAC
 ADC IP SIGNAL PROCESSING Software COMMUNICATION

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