

LXD10K0

One channel 5.4 GHz ADC with 12-bits resolution

With the LXD10K0 Logic-X provides a unique analog interface product that is based on the 12-bits low latency wide bandwidth ADC (EV12AS350A) and from Teledyne E2V. Multi card synchronization is supported thanks to a flexible clock tree and external synchronization trigger input.

Analog input

With an analog input stage that has a very wide input bandwidth from 0.5MHz up-to 4.8GHz and the low latency 5.4Gsp/s ADC from E2V (EV12AS350A) the LXD30000 delivers unmatched performance with regards to SFDR, close in phase noise and latency (7.2 ns) on its analog input channel. Sampling at 5.4 Gsp/s offers an instantaneous bandwidth of 2.7GHz.

12 bit

The ADC offers 12-bits resolution further contributing to achieve best in class signal to noise ratios.

Low Latency

It is possible to achieve a very low latency from the RF input to the FPGA fabric thanks to the LVDS connectivity to the host carrier. This can be less than 11 ns, depending on the carrier that is used.

Clock tree

The onboard low noise clock generator ensures easy integration into small single channel systems as well as standalone operation. For larger systems it is possible to directly provide the sample clock to the front panel SSMC connector or to synchronize the local clock generator to an external reference clock.

Applications

Systems that will benefit greatly from this product are

- Electronic Warfare systems
- Medical equipment
- Radar receivers
- Advanced digital radio frequency memory (DRFM) systems
- Telecommunication systems
- Many more

Key Features:

- FPGA Mezzanine Card (HPC)
- <19 ns RF to RF Latency
- 5.4 GSPS Data Rate
- 12-bit Resolution
- 0.5 to 6000 MHz Bandwidth
- LVDS signaling
- No calibration required
- Flexible clock tree
- External Trigger input and output
- System power saving options

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Specifications

Analog input

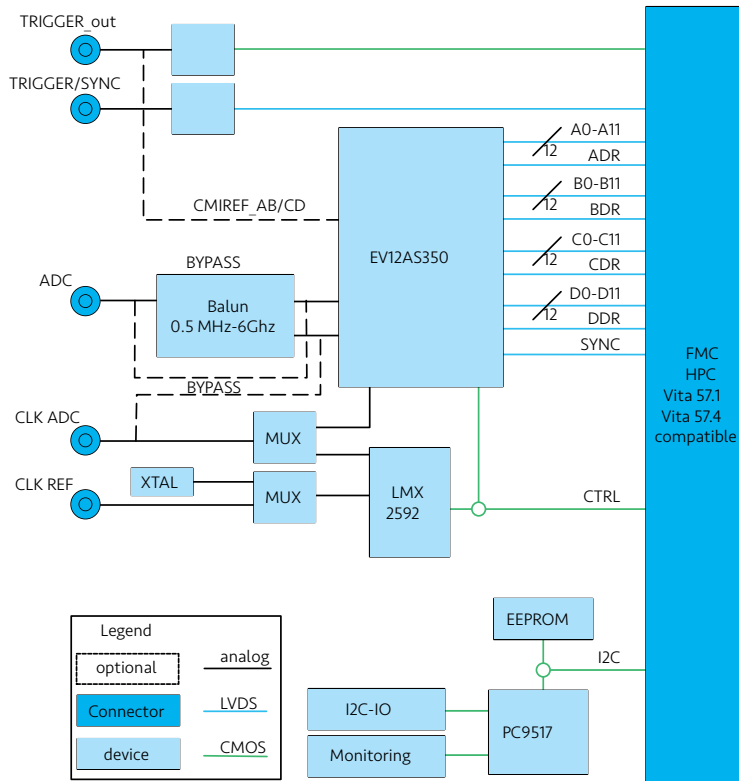
- AC coupling (differential DC optional)
- Bandwidth 0.5MHz -4.8 GHz
- Full scale Input power 8.5 dBm
- Impedance 50 Ω
- SSMC connector

Analog to Digital Conversion

- FS = Max 5.4 Gsp/s
- Data rate = Max 5.4 Gsp/s
- 12 bit
- SNR @ 1GHz 55 dBc
- SFDR @ 1GHz 60.5 dBc
- ENOB @ 1GHz 8.5 bits

Mechanical

- Vita 57.1 High Pin Count FMC
- Vita 57.4 compatible
- Convection and conduction cooled
- Max 9 Watts
- Power saving modes
- SSMC connectors



Compatible with LXF90K0



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 ADC IP SIGNAL PROCESSING Software COMMUNICATION

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