LXF33K00

Single channel 5.4 Gsps ADC and DAC with 12-bits resolution

A combination of low latency wideband analog to digital converter, digital to analog converter and Xilinx Kintex Ultrascale makes the LXF33K00 the ideal platform for embedded signal processing applications such as Electronic Warfare, Wideband Radar transceiver or wideband communication applications. The LXF33K00 is fully compliant to the Vita65.0 openVPX standard and the VITA46.11 VPX shelf management standard.

Analog input and output

With an analog input stage that has a very wide input bandwidth from 0.5MHz up-to 4.8GHz and the low latency 5.4Gsps ADC from E2V(EV12AS350A) the LXF33K00 delivers unmatched performance with regards to SFDR, close in phase noise and latency (7.2 ns). Sampling at 5.4 Gsps offers an instantaneous bandwidth of 2.7GHz. Surpassing the analog input, the analog output o?ers an even lower latency (1.2 ns) using the EV12DS460 DAC device from E2V. The output bandwidth ranges from 0.5MHz to 6GHz and the instantaneous output bandwidth is 1.35GHz. Both the ADC and DAC offer 12-bits resolution further contributing to achieve best in class signal to noise ratios.

Clock tree

The onboard low noise clock generator ensures easy integration into small single channel systems as well as standalone operation. For larger systems it is possible to directly provide the sample clock to the front panel SSMC connector or to synchronize the local clock generator to an external reference clock.

FPGA and Memory

The LXF30K00 comprises a Xilinx Kintex Ultrascale KU060 user programmable FPGA. A majority of the logic, block RAM and all DSP resources are available for customer processing. With the KU060 FPGA the LXF33K00 offers; 663 K logics cells, 1,080 36 Kbit RAM blocs, 3 PCIe interface blocks and 2,760 DSP48 slices. The FPGA speed grade is -2. The LXF3000 FPGA connects to one 72 bits wide DDR4 memory bank, offering a total of 4GB of storage with error correction codes. At 2400 Mhz the memory bank offers a total bandwidth of 21.6 GB/s. For FPGA configuration the LXF33K00 has a 64MB QSPI FLASH memory.

VPX interface

At the P1 connector the LXF33K00 has two fat pipes that form the data plane. At the expansion plane on P1 there are also two FAT pipes. Each fat pipe can be divided into two thin pipes or four ultra thin pipes. A total of thirty-two user definable LVDS signals connect between the FPGA and the VPX P2 connector. Two types of cooling are supported by the LXF33K00 For the harsher environmental conditions, the board can be ordered in the conduction cooled version. Otherwise the board is available in an air-cooled version.

Key Features:

- **VITA65.0 3U OpenVPX compliant**
- **<19 ns RF to RF Latency**
- **1240 MHz DAC update rate**
- **1 channel ADC and DAC**
- **12-bit Resolution**
- **5.4 GHz update Rate**
- **AC coupled inputs and outputs**
- **Flexible clock tree**
- **External Trigger input and output**
- **User programmable Xilinx Kintex Ultrascale KU060 FPGA**
- **4GB DDR4-2400 with ECC**
- **VITA46.11 compliant IPMI Controller**
- **Air cooled or Conduction cooled**

Applications

Systems that will benefit greatly from this product are:

- Electronic Warfare
- Radar waveform generators and receivers
- Advanced digital radio frequency memory (DRFM)
- Medical and Telecommunication

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LXF33K00 *Single channel 5.4 Gsps ADC and DAC with 12-bits resolution*

Specifications

Analog input/output
- AC coupling
- Bandwidth 0.5MHz -4.8 GHz
- Input power 8.5dBm
- Output power –5 dBm (NRZ)
- Impedance 50 Ω
- SSMC connector

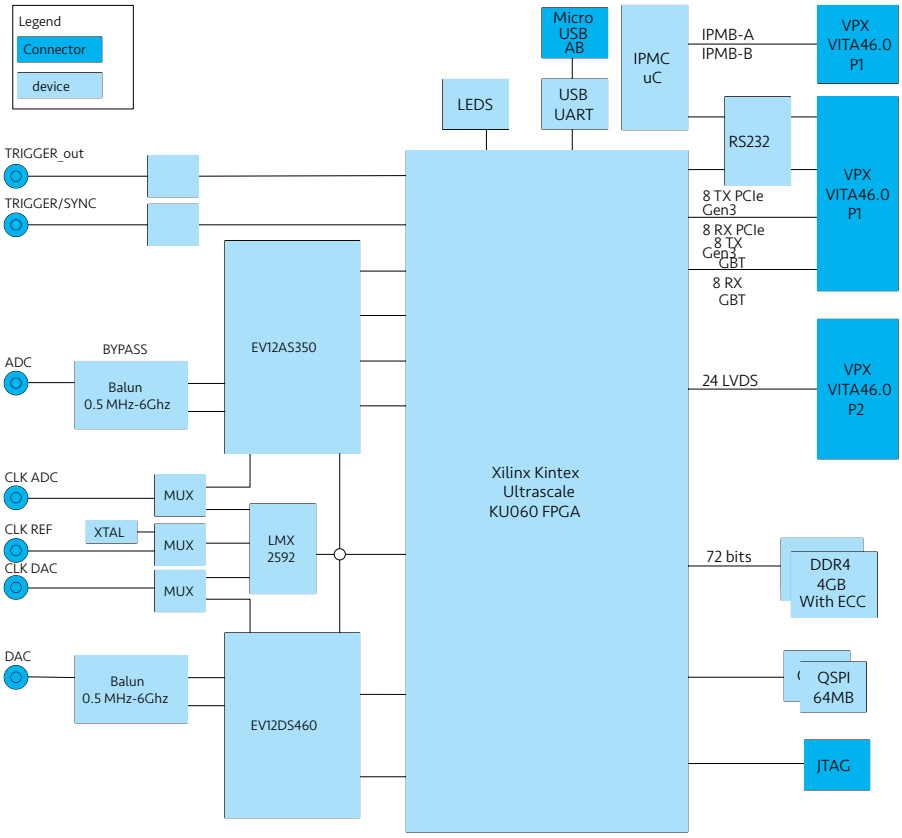
Analog to Digital Conversion
- 1 channel FS Max 5.4 Gsps
- 12 bit resolution
- SNR @ 1GHz 55 dBc
- SFDR @ 1GHz 60.5 dBc
- ENOB @ 1GHz 8.5 bits

Digital to Analog Conversion
- 1 channel FS Max 5.4 Gsps
- Data rate max 2.7 Gsps
- 12 bit resolution
- SFDR @ 1GHz 59 dBc (NRTZ)
- SFDR @ 3GHz 55 dBc (NRTZ)

FPGA
- Kintex Ultrascale KU060
- XCKU060-1FFVA1156

Memory
- 72 bits DDR4-2400
- 4GB with ECC
- 64MB QSPI FLASH

Support
- Application example for Windows
- Vivado IP integrator IP cores
- Vivado 19.0 support



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