LXD31K2

Two channels 310 Msps ADC and DAC with 16-bits resolution

The LXD31K2 provides two 16-bit A/D channels with up to 310 Msps data rate and two 16-bit D/A channels with up to 310 Msps data rate with a 1.24 Gsps update rate. All the data interfaces are based on LVCMOS and LVDS signalling. The design is based on the Analog devices AD9652 analog to digital converters and the Analog devices AD9142A digital to analog converters.

Analog input and output

Depending on the application requirements it is possible to order the LXD31K2 with either a DC coupled or an AC coupled analog front end. The DC coupled interface is meant for signal acquisitions and playback in the first Nyquist zone while the AC coupled inputs also offers the option for signal acquisition and playback in the second Nyquist zone.

16 bits

Both the ADC and DAC offer 16-bits resolution further contributing to achieve best in class signal to noise ratios.

LVDS signaling

Both the ADC and DAC device make use of LVDS signaling for their data interfaces. This allows easy integration of the LXD31K2 into user FPGA designs without the need to acquire expensive and complex JESD204B interface cores. Thanks to the low pin count implementation the LXD31K2 will work on all Xilinx development boards as well as the Logic-X FPGA FMC carrier boards.

Clock tree

The onboard low noise clock generator ensures easy integration into small single board systems as well as standalone operation. For larger systems it is possible to easily synchronize multiple boards by providing an external reference clock. This is a special feature offered by the onboard clock PLL.

Applications

Systems that will benefit greatly from this product are:

- MIMO Applications
- Digital Beam Forming
- Experimental Physics
- Analog record and playback systems
- Aerospace and test instrumentation
- Radar waveform generators and receivers
- Medical systems
- Telecommunication systems
- Software defined radio (SDR)

Key Features:

- FPGA Mezzanine (LPC)
- 2 channels DAC
- 1240 MHz DAC update rate
- 2 channels ADC
- 310 MHz ADC update Rate
- 16-bit Resolution
- AC or DC coupled
- LVDS signaling
- Flexible clock tree
- External Trigger input or output
- Advanced power monitoring
- VITA 57.1 and 57.4 compatible

LOGIC-X
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Specifications

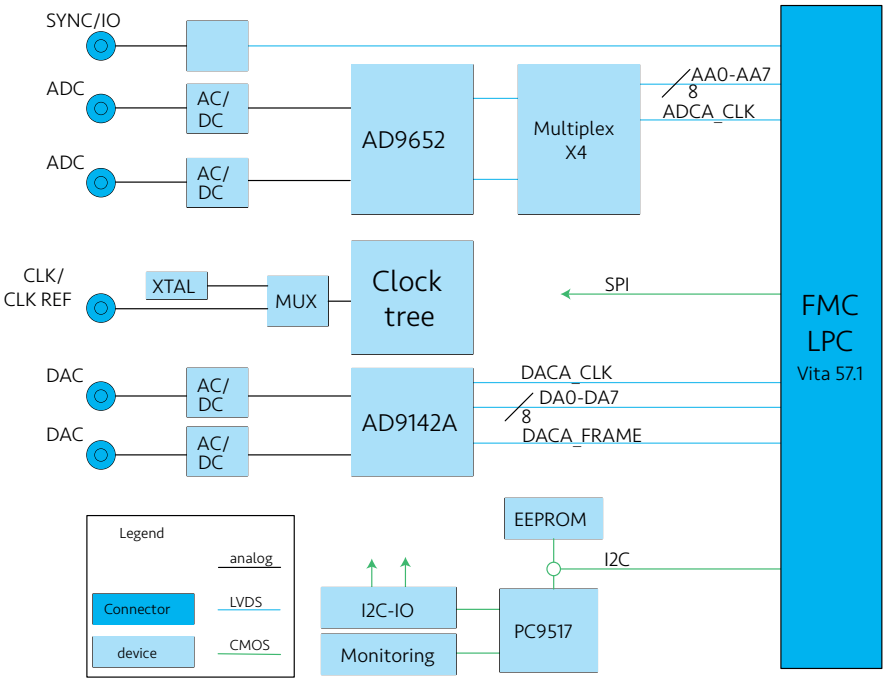
Analog input
- AC or DC coupling
- Bandwidth AC 10 MHz -400 MHz
- Bandwidth DC DC -200 MHz
- AC Full scale input power +6 dBm
- DC Full scale input power +12 dBm
- Impedance 50 Ω
- SSMC or MMCX (default)

Analog output
- AC or DC coupling
- Bandwidth AC 10 MHz -400 MHz
- Bandwidth DC DC -200 MHz
- AC Full scale output power +6 dBm
- DC Full scale output power +12 dBm
- Impedance 50 Ω
- SSMC or MMCX (default) connector

Analog to Digital Conversion
- FS = Max 310 Gsps
- 16 bits
- SNR @ 70MHz 75 dFs
- SFDR @ 70MHz 87 dBc
- SNR @ 170MHz 73.7 dFs
- SFDR @ 170MHz 85 dBc
- ENOB @ 70MHz 12 bits

Digital to Analog conversion
- FS = Max 1.24 Gsps
- Data rate =Max 310 Gsps
- 16 bit
- SFDR @ 200MHz 85 dBc

Mechanical
- Vita 57.1 High Pin Count FMC
- Vita 57.4 compatible
- Convection and conduction cooled
- SSMC or MMCX connectors



Compatible with LXF90K0