WHITE PAPER

# Game-Changing Technologies in Electronic Warfare


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# Game-Changing Technologies in Electronic Warfare


## Introduction

Electronic Warfare (EW) is the use of the electromagnetic spectrum to dominate the battlespace, deny such dominance to the foe, or to protect against attack. It is one of the most rapidly-evolving areas of technology and has come to the forefront of operations because of the advances in modern embedded computing.

The reliance of today's Command, Control, Communications, Computer, Intelligence, Surveillance and Reconnaissance (C4ISR) systems on the RF spectrum means that such systems must be prepared to meet the modern EW threat. The EW operating environment is unique because a system latency difference measured in nanoseconds can mean the difference between mission success or failure.  Low latency and jitter requirements have previously limited the system developer's range of choices when it came to both form factor and subcomponents.

This is all changing, however, as new possibilities open up for small form factor EW cards and GPGPU-based sensor processing in EW applications. It is the stated aim of the Pentagon that "In equipping our forces, we plan to develop advanced electronic attack, advanced electronic warfare support, harden our kill-chains with electronic protection and invest in electromagnetic battle management to manage the numerous assets in the battlespace". The implications span all services.

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The Air Force is planning electronic warfare upgrades for the F-15 fighter to  protect against electronic attack. The Navy is already developing its Next-Generation Jammer for the EA-18G Growler. The Army is focusing on systems to detect, locate and disrupt various signals, and have prioritized the jamming of signals that are used to trigger Radio-Controlled Improvised Explosive Devices for several years.

This paper describes how COTS technologies are pushing, and will continue to push, the frontiers of the possible in EW.

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**EW domains**
EW is not a single discipline; most current doctrines subdivide it into three:

**Electronic Attack**
– standoff EM jamming, RCIED jamming, etc. (formerly known as Electronic Counter Measures)

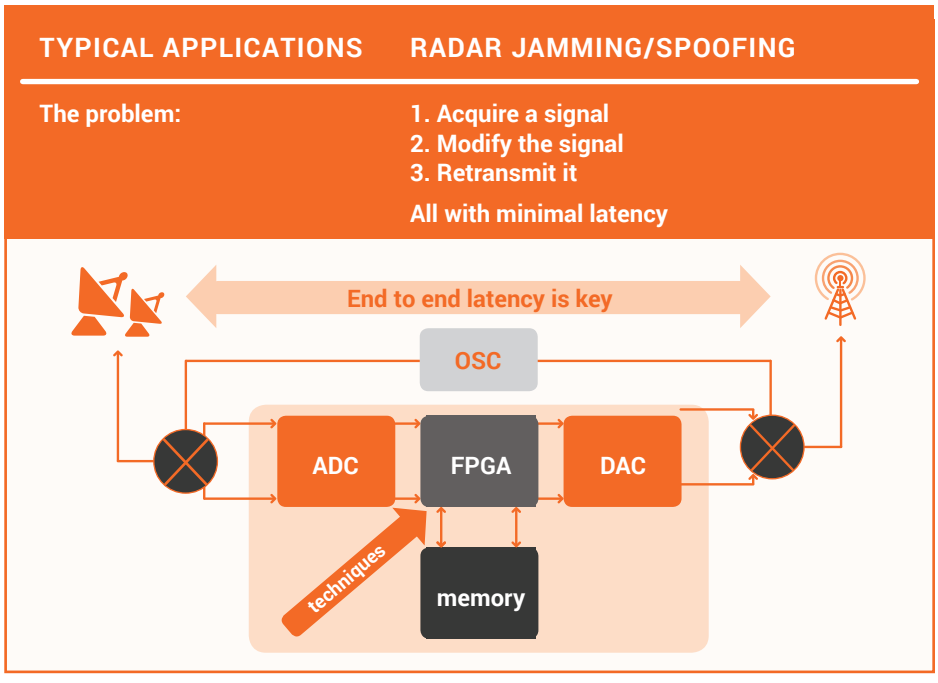
**Electronic Protection**
– hardening systems and platforms against EA (formerly known as Electronic Counter-Counter Measures)

**Electronic Warfare Support**
– the detection and classification of EM emissions that can be considered as threats, in support of EA and EP.

In no other warfare area is a clear, pre-planned product improvement technology roadmap so critical as in the EW world. As more and more modern threats emerge, EW systems must adapt or become obsolete overnight. That is why any solution must be based on state-of-the-art open systems architecture building blocks that can be both rapidly modified and implemented in both scalable and modular approaches.

**DRFM**
A common element in EW is Digital Radio Frequency Memory (DRFM). The first systems had to rely on analog electronics – delay circuits and so on - and therefore were limited in functionality, and were relatively large.

With the advent of digital technology, such systems can now be implemented in very small footprints: some complete units can be held in the palm of one hand. In a DRFM, the goal is to capture a threat signal and then replay it, usually with some modification to defeat the threat. For example, the platform under protection can be made to appear larger, or smaller, or in a different position, or with a different vector. A typical system looks like this:



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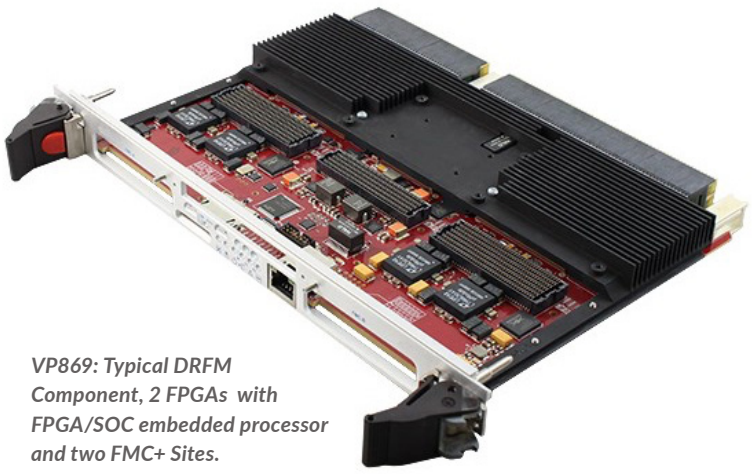
It all starts with the acquisition of a threat signal, often via a tuner, feeding into an analog-to- digital converter (ADC) and then storing that data in memory. The data is then modified in some way (known as a technique) and then is replayed from memory through a transmitter with the aim of defeating the threat. Key parameters of such circuits are latency from acquisition to replay and jitter of the timing of the modified signal with respect to the original. Certain thresholds must be met to deceive the threatening system. General purpose processors (GPPs) struggle to meet these constraints, and it is more common to see field programmable gate arrays (FPGAs) being used in these applications.

A DRFM typically features one or more acquisition ports and one or more digital-to-analog converters (DACs). It would also likely include some kind of processor that is capable of high compute power and deterministic throughput – in most cases, a high-end FPGA. These will often be Xilinx UltraScale or Intel/Altera Aria or Stratix class devices due to the demanding performance requirements. Such a system will also need a substantial amount of memory to be able to store and replay signals to keep up with acquisition speed.

FPGAs, ADCs and DACs all improve in performance over time. FPGAs broadly follow Moore's Law as they leverage the same fabrication and node technologies as GPPs. ADCs and DACs have other figures of merit – sample rate, effective number of bits (ENOB), and power, that improve over time too. Because they follow their own timelines, it is desirable to decouple the processor from the ADC and ADC at the hardware level to allow independent upgrades. An enabling factor here is the use of FPGA Mezzanine Cards (FMCs). FMC is an ANSI and VITA standard that defines mezzanine modules (such as ADCs and DACs) with high speed connections to an FPGA or other device on a carrier board.



*VP869: Typical DRFM Component, 2 FPGAs with FPGA/SOC embedded processor and two FMC+ Sites.*

Recent advances in general purpose computing on graphics processing units (GPGPU) technology have opened new possibilities for their use in some EW applications. There has long been interest in using GPUs as processing elements in radar and other applications where latency and ruggedization were not primary constraints.

In the past, DRFM systems were only available in larger form factors that limited their use. However, Abaco has the ability to compress this technology into small form factors, including 3U OpenVPX. The smaller size allows the use of DRFM systems in SWaP-optimized end applications, such as deployment in pods underneath fighter jets or on small unmanned vehicles.

### Latency

One key characteristic when selecting an FMC for an EW application (beside the obvious – sample rate, ENOB, etc.) is the latency inherent in the interconnect from ADC to FPGA. In many newer ADCs and DACs, this can be a JESD204B link.

JESD204B is a variable lane width serial link with 8b10b encoding and an embedded clock that is attractive as it can reduce the trace count when compared to LVDS links (much as PCI Express superseded PCI). However, the process of serializing and de-serializing the data inserts latency in the path, which is undesirable in these applications. The system designer must consider the end-to-end latency: for the receive path, this is the latency of the ADC itself, the serializer in the ADC, the lane delay, the de-serializer in the FPGA, and the elastic buffer that is normally needed.

This entire path is the sample-to-parallel-out latency that the application must tolerate. In many EW uses, this figure must be in the sub 100 nanosecond range, something not typically achievable with current serial paths. There is some optimism that new standards such as JESD204C will address this, and there is anticipation that high speed ADCs and DACs will soon be integrated into the same die as high end FPGAs, yielding tighter coupling at low latency. For today, however, parallel paths remain the preferred option. The tradeoff here can be the number of channels that can be accommodated due to the limited number of pins available on the FMC connectors.

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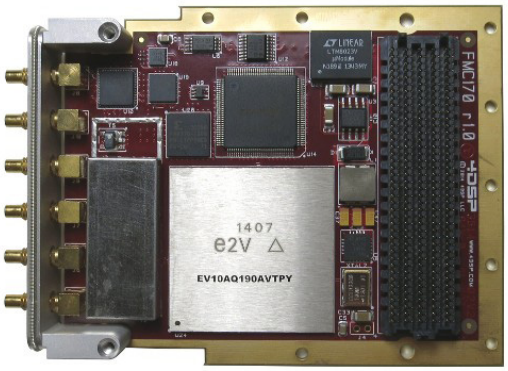
Another area where latency can creep into the system, especially where the phase data of a signal is important - such as direction finding - occurs when signals are sampled in the real domain and the phase data is extracted via a Hilbert Transform – a costly mathematical operation. This can be avoided if the ADCs selected can be synchronized across multiple channels with minimal timing jitter to allow meaningful I/Q sampling.

Abaco has a large selection of FMCs in the 4DSP portfolio, some with JESD204B, some with LVDS, allowing selection of the most appropriate link for the use case. Modules with sample rates from 65Msps to 5Gsps are available, as are clock generation and distribution schemes to allow for the critical timings needed for coherent operation.




*FMC170: High-speed, Wide-band, 5GSPS, Low Latency Electronic Warfare Analog I/O FMC ideal for electronic warfare DRFM applications.*

## GPGPU Processing

Recent advances in general purpose computing on graphics processing units (GPGPU) technology have opened new possibilities for their use in some EW applications. There has long been interest in using GPUs as processing elements in radar and other applications where latency and ruggedization were not primary constraints. The compelling reason for looking to GPUs is their raw processing rate as well as the GigaFLOPS per watt metric for those customers who have significant power limitations. GPUs can also be compelling when stacked up against FPGAs because application engineers appreciate the ability to program GPUs in C or C++ derivative languages rather than having to use VHDL, as FPGAs require. GPU programmers can typically turn around new algorithms much more quickly, saving time and development costs.

In the past, there have been two objections to using GPGPU technology in applications such as EW: the relatively low levels of ruggedization available, and the latency disadvantage when compared to FPGAs. However, Abaco Systems has been able to solve the ruggedization issue through its relationship with NVIDIA. Abaco offers fully ruggedized, chip-down GPGPU products that carry full lifecycle support and can be deployed today in real world military applications.

> A mixed environment of FPGAs, GPUs and the latest multicore system-on-chip (SoC) GPPs allow different processing chains to be applied to the same acquired data for different purposes, each using the most appropriate architecture for the use case.

As for objections related to latency – which were certainly valid – the advent of GPUDirect RDMA has mitigated this, enabling GPGPU technology to fulfill its unquestioned potential. This allows data from an endpoint (eg. an FPGA sitting behind an ADC) to DMA data straight to GPU memory, bypassing legacy bottlenecks in system memory. This results in a reduction of latency from acquisition to processing of one to two orders of magnitude. While this does not approach the levels achievable with FPGAs, it does mean that GPUs start to become viable for some aspects of EW that were previously out of reach.

## Convergence

With the move to Active Electronically Scanned Arrays (AESAs), many radars are becoming multifunction, combining scanning, tracking, imaging and more. In addition, due to the bandwidth and beamforming capabilities of the arrays, radar is being combined with other functions, such as Electronic Attack and Communications.

The same aperture and processing systems are being tasked with multiple functions that were once fulfilled by multiple, federated systems. Add to this the need for cognitive radar and EW processing driven by the need to generate new and novel waveforms by the former, and the need to counter these by the latter and it is easy to understand the emergence of heterogeneous processing systems. These mix FPGAs, GPUs and the latest multicore system-on-chip (SoC) GPPs, allowing different processing chains to be applied to the same acquired data for different purposes, each using the most appropriate architecture for the use case.

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*The VPX167, a 3U VPX airborne pod platform with up to seven slots.*

For instance, FPGAs excel at parallel throughput and determinism, but struggle with the decision making and branching that come along with cognitive techniques. Here, x86 SoCs may fare better.

An example of such a system is the Abaco VPX167, a 3U-based VPX system designed to be embedded in many pod types flown by the US military. With up to five 3U VPX slots, the VPX167 offers a high performance and modular architecture in a small and ruggedized form factor suitable for the most demanding EW applications.

A single board computer (SBC) will typically act as the control and communication hub and connect to multiple peripheral cards. Subsystems with the following components and capabilities are possible: RF down- and up conversion, switched filter banks, analog-to-digital, digital-to-analog, FPGA and DSP capabilities.

The slim, light-weight and yet extremely powerful system is made possible thanks to advances in the miniaturization of high end digitizers, waveform generators and associated processing units that can be reconfigured to fit the demands of specific missions. With a flexible architecture that relies on commercial off-the-shelf (COTS) modules, the VPX167 cuts down integration time and ensures determinism when there is no margin for error.

The VPX167 can host a variety of COTS-based systems that are a combination of custom RF systems, COTS processing cards and custom, reconfigurable firmware. Example SBCs include SBC328 and SBC347D – quad core Xeon E3 6th Gen Intel Core and quad-to-sixteen Intel Xeon D processors respectively. FPGA board choices include VP780 with Xilinx Virtex 7 (UltraScale on the way). A wide range of ADC and DAC FMCs can be selected, as can GPGPU accelerators like the GRA113.

The combination of FlexVPX backplanes and COTS VPX modules allows the flexibility to configure the board set that best meets the needs of the application, and enables rapid technology insertion to address future obsolescence or change of scope in functionality without redesigning the entire system, leading to significant reductions in engineering costs and schedules.

### Security

In a world in which the protection of intellectual property and critical program information is becoming increasingly important, nowhere is the need more acute than in EW systems. Consideration must be given to how to protect sensitive data at rest, data in use and data in transit. Here, the selection of COTS modules that incorporate protection, and more importantly the selection of a COTS vendor that understands the needs and can act upon them is critical. From trusted boot to support for multiple independent levels of security (MILS) operating systems, Secure Hypervisor, and middleware products, Abaco is ready to support these needs.

## Conclusion

EW technologies will continue to evolve rapidly on both the offensive and defensive sides of the equation. Where the unique demands of the domain once made the most high-performance commercial products less suitable for EW, recent advances in DRFMs, SoCs and GPUs have reduced the SWaP needs of EW systems and increased their performance potential.

Abaco Systems is at the leading edge of such developments and will continue to bring the best commercial technologies to the military and aerospace market where they can help customers increase capability, mitigate program risk, and lower total cost of ownership - all from a trusted long term supplier.

WE INNOVATE. WE DELIVER. YOU SUCCEED.

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