Leveraging FPGAs for Evolving ISR Application Requirements

HALEY TECHNOLOGY
和澄科技股份有限公司
www.haleytech.com sales@haleytech.com
新竹+886-3-579-0380 Fax : +886-3-579-0370

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Introduction

The increasing demand for embedded computing systems to power intelligence, surveillance, and reconnaissance (ISR) applications on unmanned aerial vehicles (UAV) is driving the need for the rapid development and deployment of reconfigurable COTS (commercial off-the-shelf) hardware platforms that combine high performance and flexibility. These solutions allow for application-specific product customization, as well as increased design flow automation which enables DSP engineers to leverage the parallel processing capabilities of the FPGA to boost performance and improve the cost benefits of the platform.

Flexible FPGA-based systems also make lower size, weight, and power (SWaP) profiles possible to better suit UAV airframes while delivering higher computational density for ISR applications when compared to other types of systems based solely on general purpose processors (GPPs). Signals intelligence (SIGINT) tasks such as wideband signal acquisition and analysis are now performed on unmanned aircraft using the high performance and low latency FPGA-based approach. In the past, such functions were executed on the ground because the bulky and power-hungry systems they require exceeded the SWaP limitations of UAVs.

Significant advances in performance and SWaP efficiency are being delivered by the newest generation of FPGAs, including Xilinx's UltraScale families, which have significantly improved processing performance per watt, enabling smaller, more power-efficient platform designs for compute-intensive ISR applications. In airborne applications, high-end FPGAs are particularly useful for interfacing to sensors and moving large amounts of data. They can also be used to interface with legacy I/O devices by allocating some I/O pins and logic on the FPGA to translate the legacy I/O protocol.

> Reconfigurable hardware based around the FPGA is essential for the rapid deployment of UAV payloads.

Opportunities

Reconfigurable hardware based around the FPGA is essential for the rapid deployment of UAV payloads because it is possible to program application-specific algorithms that benefit from high computational efficiency exceeding that of general-purpose devices such as CPUs or GPUs. A modular system also improves scalability and provides more opportunities for code reuse. Modular software design enables proven IP to be repurposed for multiple ISR applications, while modular hardware configurations ease the scaling of an ISR application to better meet the requirements of a mission and the SWaP profile of the UAV airframe.

These characteristics help to speed deployment of UAV applications and further lower costs by shortening the development cycle and improve system reliability by minimizing the number of field failures.

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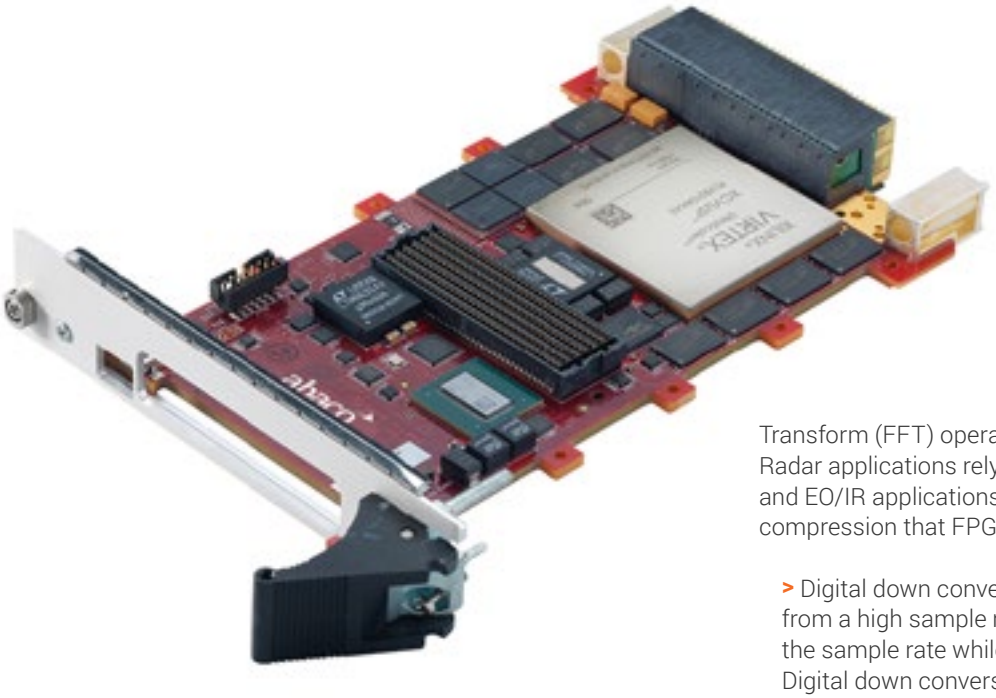

The VP889 3U VPX with a Xilinx Virtex Ultrascale+ is ideal for ISR DSP applications that require a flexible architecture to adapt as requirements change.

FPGAs for Sensor Processing

The UAV now plays a key role in the delivery of detailed data for a wide range of defense operations. The need for greater signal processing capability on UAV platforms is a result of the rapid evolution and expansion of ISR and SIGINT duties taken on by UAVs and the increasing sensitivity of their onboard sensors, including advanced antennas, as well as electro-optic (EO) and infrared (IR)-capable cameras.

It is therefore essential that the embedded sensor processing subsystems that must contend with the greatly increased volumes of data being collected by these sensors take advantage of both the parallel computing resources offered by low power and efficient FPGAs and the capabilities of modern ADCs packaged in small form factors such as the FPGA Mezzanine Card (FMC – VITA 57.1/57.4). When combined with high performance wideband or GHz-capable analog-digital converters (ADCs), FPGAs are essential to digitizing the analog input from a sensor and then processing the acquired bitstream.

The sensor processing functions performed by FPGAs can be divided into a few general categories. For SIGINT applications, digital down conversion is used for narrowband extraction in the time domain, while data reduction and tuning with Fast Fourier Transform (FFT) operations are used in the frequency domain. Radar applications rely on pulse compression and equalization, and EO/IR applications benefit from the very efficient image compression that FPGAs can perform.

> Digital down conversion mixes a band-limited digitized signal from a high sample rate to a lower frequency and reduces the sample rate while retaining the target data information. Digital down conversion thereby enables the digital extraction of a high-fidelity narrowband signal out of a broader spectral window. The primary advantage of using an FPGA for digital down conversion is the real-time parallel processing speed of its configurable logic blocks. FPGAs also provide developers with great flexibility when implementing digital down conversion if, for instance, the characteristics of the filter need to be changed and the coefficients reconfigured.

> Data reduction and tuning also benefit from the parallelism and flexible programming provided by FPGAs. The performance of FFT operations is greatly improved by the dedicated DSP logic within FPGAs when performing frequency binning. UltraScale FPGAs from Xilinx feature logic that is central to both the filtering and the FFT algorithms.

> FPGAs are also ideal for implementing the series of three operations — FFT, complex multiply, and inverse FFT — that typically enable pulse compression for radar signals. The parallelism of FPGAs can be used to efficiently apply equalization to the signals acquired from an array of antennas in a radar system, with each element of the array feeding a separate input channel to a DSP with a high bandwidth link to the FPGA.

> The data stream from the sensor to the FPGA in EO/IR applications can be overwhelming for data management and storage resources due to the size of digital images generated. Efficient image compression or data reduction is therefore required, and FPGAs are well suited for the algorithms commonly used for this purpose.

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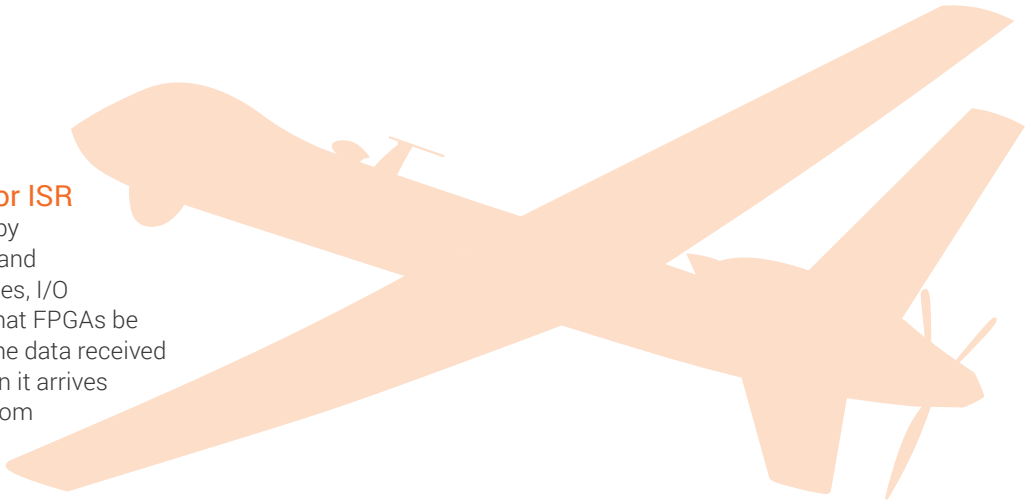

Deploying FPGA-Based Systems for ISR

The low level processing tasks performed by FPGAs are similar for various applications and systems, but the wide variety of sensor types, I/O options, and platform constraints dictate that FPGAs be configured in many ways. For example, if the data received from an antenna is still in analog form when it arrives at an FPGA module, the preferred design from the signal integrity and performance perspective suggests that the ADC components be placed near the FPGA with high bandwidth connections. In other scenarios, the ADC may need to be positioned closer to the antenna, and the input to the FPGA module will already be digitized, such as in EO/IR applications where the sensor's digitized data stream must be connected directly to the FPGAs.

The size of the vehicle platform is also a key consideration. Large platform applications, such as seafaring vessels or manned aircraft, can be outfitted with large and very powerful 6U systems for processing data collected by sensors. Some UAV platforms such as the Predator are also large enough to support 6U systems, but most other UAVs are smaller and, therefore, better candidates for compact 3U systems, particularly those based on the OpenVPX standard (VITA 65). The 3U form factor was originally used in UAVs mostly for mission computers and less intensive ISR and SIGINT applications, but that has changed as computing power on 3U boards has increased.

FlexVPX backplane with multiple configurations available.

This has, of course, raised heat density and made the management of cooling and the development of adaptive power reduction techniques very important. There are other options for designing FPGA-based solutions, but the interoperability, high bandwidth capacity, and ruggedization levels possible with OpenVPX have led to this standard's wide adoption in the defense industry.

Abaco Solutions for ISR

There are a number of ways of implementing advanced FPGAs to serve the needs of airborne ISR processing applications. A flexible FPGA-based architecture in a 3U VPX form factor such as Abaco's VP889 can be combined with the latest in wideband ADCs and high-speed, high-resolution DACs on FMC modules. FMCs from Abaco's extensive portfolio can be selected as needed to build an ultra-high-speed digital transceiver to handle both low-latency signal processing in either air or conduction-cooled configurations while also handling data movement functions. Such a configuration offers a high level of flexibility, as subsystems can be simply upgraded over time with new technology as it becomes available.

For these small form factor systems to become even more suitable for UAVs, new 3U VPX backplane topologies are required as many of today's 3U designs are unable to fully exploit the high bandwidth made available by the most advanced FPGAs. Given the strict size restrictions inherent in small and medium-sized UAV airframes, it is also extremely important that these subsystems be able to adapt to compact environments. Abaco has addressed these challenges with its FlexVPX line of VPX backplanes which offers the ability to interconnect two and three-slot 3U VPX-compliant backplanes.

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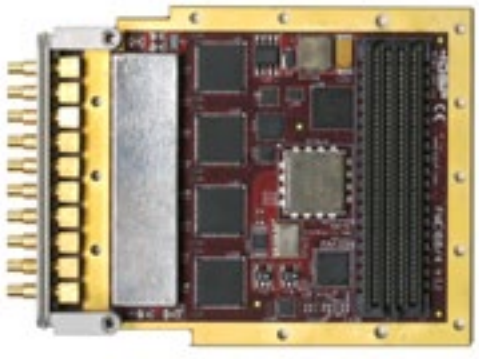

FMC168 Caption: FMC168 very wideband, high resolution ADC FMC is a critical component in ISR systems.

This opens new options for embedded computing designs for UAVs by allowing greater customization using COTS hardware.

Developed in collaboration with a large research laboratory, FlexVPX addresses SWaP concerns by subdividing a larger backplane format into smaller boards that maintain a high speed data path using multi-port PCI Express bridges, ensuring high throughput for point-to-point communication between different elements in the system. High speed cables plug directly into the rear side of the backplanes, enabling backplane-to-backplane communication with tens of Gigabits throughput. In this way, FlexVPX backplanes deliver the functionality of larger traditional backplanes in a modular form factor that can be used to deploy mission-critical embedded computing functions within very limited physical spaces, such as those found on most UAVs.

Conclusion

UAVs continue to assume a greater role in strategies to help reduce and support global troop commitments by expanding surveillance and intelligence gathering while keeping costs in check. As a result, program managers are understandably emphasizing the improvement of payload technology for ISR missions.

One example of this is the growing need for the ability to geo-locate targets when using synthetic aperture radar (SAR) systems combined with EO/IR imaging to improve tactical responses to SIGINT data. These are compute-intensive applications, so payload designs must respond accordingly to deliver greater real-time signal processing capacity. This is where standardized system-level architectures like VPX, coupled with advanced FPGAs, can bring performance gains to ISR payloads by reducing cost and complexity. VPX gives application engineers and systems integrators an adaptable solution that puts computational resources closer to the sensors.

To address these considerable challenges, Abaco is continuously innovating in several standard (including PCIe, VPX, and FMC) form factors to bring the best embedded COTS solutions to market for executing the complex processing tasks required by the next generation of UAVs.

WE INNOVATE. WE DELIVER. YOU SUCCEED.

Americas: 866-OK-ABACO or +1-866-652-2226 Asia & Oceania: +81-3-5544-3973
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